Electronic Version
Stylesheet Version v1.1.1

LOW TRIGGER VOLTAGE ESD NMOSFET TRIPLE-WELL CMOS DEVICES

Abstract

An ESD NMOSFET, and a method for lowering a ESD NMOSFET trigger voltage. An ESD NMOSFET is configured in triple well CMOS architecture where the first well is separated from second and third wells by respective shallow well isolation regions. The first well is also separated from the substrate along the bottom by a conductive band region. A substrate contact is located outside of the first, second and third wells, and provides a current path during an ESD event from the first well. Source and drain regions are formed in the first well, to form an FET with the drain being connected to an I/O pad which is subject to an ESD event. A resistive path extends through an opening in the conductive band region to a substrate contact, providing an increased I/O pad to substrate resistance which decreases the trigger voltage for the ESD NMOSFET.